under a selected gate bias. An internal gate structure **916** of MOSFET **920** is formed adjoining doped region **921**. In some embodiments, internal gate structure **916** has a similar structure to first and second internal conductor structures **911** and **913**. In some embodiments, internal gate structure **916** includes a trench **39** lined with insulating layer **41** and having a trench conductor **43**. One difference is that internal gate structure **916** includes gate dielectric layer **926** separating trench conductor **43** from doped region **921**. In some embodiments, gate dielectric layer **926** is silicon oxide or other gate materials used in MOSFET devices. In some embodiments, gate dielectric layer **926** is thinner than insulating layer **41**. In one embodiment, a portion **81** of insulating layer **31** on major surface **28** on the surface near the HEMT gate is extended to cover another end of the trench conductor **43** in internal gate structure **916**. In some embodiments, electrical contact is made to trench conductor **43** in internal gate structure **916** in another portion of device **90** (not shown).

FIG. **9** illustrates an enlarged cross-sectional view of an embodiment of a multi-transistor device **100** that is an alternate embodiment of device **90** illustrated in FIG. **8**. Device **100** is similar to device **90** but has a different conductivity type of MOSFET **930**. In some embodiments, substrate **11** in device **100** includes a p-type substrate instead of the N-type substrate of device **90**. In some embodiments, a portion of substrate **11** below internal gate structure **916** functions as the channel region of the MOSFET. Device **100** also includes a first doped region **927** of an opposite conductivity type (opposite to the substrate type, for example, n-type) formed in the substrate to function as the source region of MOSFET **930**. Another doped region **923** of the opposite conductivity type to substrate **11** is formed to function as the drain of MOSFET **930** and the source of HEMT device **910**. The gate of the MOSFET is formed as a gate structure similar to the gate structure of device **90** except that the gate structure adjoins a channel region of the substrate instead of a channel region formed by a doped region formed in the substrate. In some embodiments, first conductor **372** is isolated from gate electrode **27** by insulative layer **31** in first internal conductor structure **911**.

From all of the foregoing, those skilled in the art can determine that according to one embodiment, a method of forming a semiconductor device can comprise providing a base substrate of a first semiconductor material (for example, element **11**) wherein the base substrate defines a first current carrying electrode of the semiconductor device; forming III-nitride channel layer (for example, element **19**) on the base substrate; forming a III-nitride barrier layer (for example, element **21**) on the channel layer; forming a second current carrying electrode of the semiconductor device in the barrier layer; forming a gate (for example, element **27**) of the semiconductor device overlying a portion of the barrier layer and spaced apart from the second current carrying electrode; and forming a first internal conductor structure (for example, element **38**) extending from the barrier layer through the channel layer to the base substrate wherein the internal connector structure forms a low resistance vertical electrical current path from the base substrate to the barrier layer.

In another embodiment, the method can include forming the internal conductor structure to electrically connect to the base substrate and to the barrier layer.

A further embodiment of the method can include forming a first conductor within the barrier layer and forming a second conductor extending from the first conductor to the base substrate and forming an insulator between the second conductor and the channel layer.

In another embodiment, the method can include forming a Schottky barrier connection between the first conductor and the barrier layer.

In another embodiment, the method can include forming the internal conductor structure to electrically connect to the base substrate and to a major surface of the barrier layer.

In a further embodiment, the method can include forming a first doped region of a first conductivity type in the base substrate and spaced apart from the first internal conductor structure wherein the first conductivity type is opposite to a conductivity type of the base substrate; forming a gate conductor of a MOS transistor overlying the first doped region wherein a portion of the first doped region forms a channel region of the MOS transistor; forming a second internal conductor structure adjacent to but spaced apart from the first doped region, the second internal conductor structure extending from the barrier layer through the channel layer to the base substrate wherein the internal connector structure forms a low resistance electrical current path.

Another embodiment of the method can include forming a first current carrying electrode of the MOS transistor as a portion of the base substrate underlying the first internal conductor structure.

In another embodiment, the method can also forming an electrical path between the gate and the second internal conductor structure to form a low resistance electrical connection from the gate to the base substrate wherein a portion of the base substrate underlying the second internal conductor structure forms a first current carrying electrode of the MOS transistor.

Another embodiment of the method can include forming a first doped region of a first conductivity type in the base substrate and abutting the first internal conductor structure wherein the first conductivity type is opposite to a conductivity type of the base substrate and wherein the first doped region forms a first current carrying electrode of an MOS transistor; forming a second doped region of the first conductivity type in the base substrate and spaced apart from the first doped region wherein the second doped region forms a second current carrying electrode of the MOS transistor; forming a gate conductor of the MOS transistor overlying a portion of the base substrate that is between the first and second doped regions wherein the portion of the base substrate forms a channel region of an MOS transistor; forming a second internal conductor structure extending from the barrier layer through the channel layer to the second doped region wherein the internal connector structure forms a low resistance electrical current path.

In another embodiment, the method can also include forming an electrical path between the gate and the second internal conductor structure to form a low resistance electrical connection from the gate to the second current carrying electrode of the MOS transistor.

Those skilled in the art will also appreciate that another embodiment of a semiconductor device can comprise a semiconductor substrate (for example, element **11**) of a first conductivity type, wherein the semiconductor substrate provides a first current carrying electrode of the semiconductor device; a plurality of III-nitride layers (for example, elements **16**, **17**, **19**, **21**) on the semiconductor substrate to provide an HEM structure; and an internal conductor structure (for example, element **38**) extending from a major surface (for example, element **28**) of the HEM structure to the semiconductor substrate providing a vertical current path from the semiconductor substrate to the HEM structure.

Another embodiment can include an epitaxial layer between the conductive substrate and the plurality of III-